CLAIMS

What is claimed is:

1. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a stoichiometric Ga_2O_3 gate oxide layer positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said stoichiometric Ga_2O_3 gate oxide layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas.

2. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the stoichiometric Ga_2O_3 gate oxide layer forms an atomically abrupt interface with the upper surface of the compound semiconductor wafer structure.

3. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the stoichiometric Ga_2O_3 gate oxide layer has a thickness of 20 - 200 Å.

4. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the Ga_2O_3 gate oxide layer protects the upper surface of the compound semiconductor wafer structure.

5. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim

1 wherein the refractory metal gate electrode comprises a refractory metal which is stable in presence of a Ga_2O_3 gate oxide layer at an elevated temperature of 700 °C and above.

6. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the refractory metal gate electrode comprises a refractory metal selected from the group consisting of W, WN or WSi or combinations thereof.

7. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprise Sisaid enhancement mode metal-oxide-compound semiconductor field effect transistor being an n-channel device.

8. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprise and Be/F, said enhancement mode metal-oxide-compound semiconductor field effect transistor being a p-channel device.

9. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein dielectric spacers are positioned on sidewalls of the stable refractory gate metal electrode.

10. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer.

11. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim

10 wherein the wider band gap spacer layer is positioned between the gate oxide layer and the narrower band gap channel layer.

12. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 11 wherein the wider band gap spacer layer has a thickness of between 3 - 200 Å.

13. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 11 wherein the wider band gap spacer layer comprises either $Al_xGa_{1-x}As$ or $In_zGa_{1-z}P$ or a combination thereof.

14. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 13 wherein the narrower band gap channel layer has a thickness of 10 - 300 Å.

15. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 10 wherein the narrower band gap channel layer is positioned between the wider band gap spacer layer and a buffer layer.

16. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 15 wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$.

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~~17~~. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the upper surface of the compound semiconductor wafer structure comprises GaAs.

~~18~~. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim

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1 wherein the compound semiconductor wafer structure comprises a $Al_xGa_{1-x}As$, $In_yGa_{1-y}As$, or $In_zGa_{1-z}P$ layer, said layer being positioned on upper surface of a compound semiconductor substrate.

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~~19~~. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 17 ~~18~~ wherein the compound semiconductor substrate includes a GaAs based semiconductor wafer.

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20. A method of fabricating an enhancement mode metal-oxide-compound semiconductor field effect transistor comprising the steps of:

providing a compound semiconductor wafer structure having an upper surface;

depositing a stoichiometric Ga_2O_3 gate oxide layer on upper surface of said compound semiconductor wafer structure;

positioning a stable refractory gate metal on upper surface of said stoichiometric Ga_2O_3 gate oxide layer;

providing source and drain ion implants self-aligned to a gate electrode; and

positioning source and drain ohmic contacts on ion implanted source and drain areas.

21. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein the step of providing a compound semiconductor wafer structure includes the step of preparing an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure.

22. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein the step of depositing the stoichiometric Ga_2O_3 gate oxide layer comprises thermal evaporation from a crystalline Ga_2O_3 source on an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure.

23. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein the stoichiometric Ga_2O_3 gate oxide layer functions as an etch stop layer protecting the upper surface of the compound semiconductor wafer structure from gate oxide during and after gate metal etching.

24. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein the stable refractory gate metal refrains from reacting with or diffusing into the stoichiometric Ga_2O_3 gate oxide layer during high temperature annealing of the source and drain ion implants.

25. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein an interface formed by the stoichiometric Ga_2O_3 gate oxide layer and the upper surface of the compound semiconductor structure is preserved during high temperature annealing of the source and drain ion implants.

26. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 further comprising the step of annealing the source and drain implants at approximately 700 °C using rapid thermal annealing.

27. A method of fabricating a metal-oxide-compound semiconductor field effect transistor as claimed in claim 20 wherein the source and drain implants are realized by positioning dielectric spacers on sidewalls of the stable refractory gate metal.

28. A method of fabricating an enhancement mode metal-oxide-compound semiconductor field effect transistor (FET) comprising the steps of:

providing a compound semiconductor wafer structure having an atomically ordered and chemically clean upper surface;

depositing, by thermal evaporation from a crystalline Ga_2O_3, a stoichiometric Ga_2O_3 gate oxide layer on upper surface of said compound semiconductor wafer structure;

positioning a stable refractory gate metal on upper surface of said stoichiometric Ga_2O_3 gate oxide layer;

providing source and drain ion implants self-aligned to a gate electrode;

annealing the source and drain implants at approximately 700 °C using rapid thermal annealing; and

positioning source and drain ohmic contacts on ion implanted source and drain areas.